1) Event driven, time driven, and cycle based, with their relative speeds in that order from slowest to fastest. Cycle based, it only does functional simulation

5)

Entity function is

Port(a,b,c : in std\_logic;

Y : out std\_logic);

End function

Architecture boole of function is

Begin

Y<= (a and b) or c;

End boole

Architecture selected of function is

Begin

With (a&b&c) select

Y<= ‘1’ when “001”| “011” | “101” | “111”| “110”;

‘0’ when others;

End selected;

Architecture condition of function is

Signal temp : std\_logic\_vector(2 downto 0);

Begin

Temp <= a&b&c;

Y<= ‘1’ when “001”| “011” | “101” | “111”| “110” else

‘0’;

End condition;

6) see attached

11) When a signal is assigned given multiple signal assignments concurrently.

12) Suspended: Nothing is happening in the simulation  
 Active: In the active process queue, but not running yet  
 Running: Being run

13) Time is set to 0 and all processes are put in the queue. All processes in the queue are run, with their next updates being scheduled at future times. Once all processes are run, they are suspended and initialization complete.

15) Attached

19) Attached

22) If a signal is assigned in two separate processes, it is assigned concurrently with potentially different values. If it is assigned two different values, the result is indeterminate.